UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/256,265	02/23/1999	DAH-BIN KAO	16405-311	9612

25696 7590 03/14/2003

OPPENHEIMER WOLFF & DONNELLY
P. O. BOX 10356
PALO ALTO, CA 94303

EXAMINER
DIAZ, JOSE R

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 03/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/256,265	KAO ET AL.	
	Examiner	Art Unit	
	José R Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,8-10 and 16-22* is/are pending in the application.

4a) Of the above claim(s) *18-22* is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,16 and 17* is/are allowed.

6)☒ Claim(s) *8-10* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

➢ A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on December 28, 2002 has been entered.

Election/Restrictions

➢ Applicant's election with traverse of Species I in Paper No. 22 is acknowledged. The traversal is on the ground(s) that each of claims 1, 8 and 16 of the present application reads on, and is generic to, the subject matter depicted in Figure 2. This is not found persuasive because Species I and II are patentable distinct species. In fact, nowhere in claims 1, 8 and 16 Applicant uses the term "at least one", as now argued by Applicant, or claims more than one floating gate. In fact, each claims 1, 8 and 16 specifically recites only one floating gate (see claim 1, line 6; claim 8, line 2, and claim 16, line 6, wherein the phrase "a floating gate" is used). Thus, claims 1, 8 and 16 do not require an additional floating gate. As matter of fact, Figures 1 and 2 support this assertion. For instance, Figure 2 shows an erase gate located between two floating gates such that the erase gate extends over a sidewall and a portion of the top of each floating gates and over the source region. However, Figure 1 only requires one floating

gate such that an erase gate is located over a sidewall and a portion of the top of such a floating gate. Therefore, claims 1, 8 and 16 are not generic to the subject matter depicted in Figure 2, since claims 1, 8 and 16 does not require a second floating gate as needed in Figure 2. As such the restriction is considered to be proper.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

➢ The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

➢ Claims 8-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Eitan et al. (US Patent No. 4,998,220).

Regarding claims 8-9, Eitan et al. teach a memory array comprising: a substrate (103) having a channel region (107a) (see Figs. 5 and 7a and Abstract); a first insulating layer (consider portion of the layer 105a, which is between the floating gate 104a and the channel region 107a); a floating gate (104a), a second insulating layer (consider portion of the layer 105a, which is on top of the floating gate 104a and between the control gate 106 and the erase gate 108); a control gate (106) having a portion disposed over a portion of said channel region (107a) and being separated therefrom by said second insulating layer, and wherein a portion of said control gate is disposed in facing relationship to a side surface of said floating gate and is separated from said floating

gate by said second insulating layer (see Fig. 7a and Abstract), an erase gate (108) formed over one of the sides of said floating gate (104a) and being separated by said second insulating layer (see Fig. 7a), a drain region (102a), a source region (110), (see Figs. 5 and 7a and Abstract); a plurality of rows and columns (see Fig. 5) of interconnected memory cells wherein the control gates are connected by a common word line (106) (see Fig. 5), the erase gates are connected by a common erase line (108) (see Fig. 5), the source regions are connected by a common source line (110) (see Fig. 5), and the drain regions are connected by a common drain line (see col. 6, lines 55-58); whereby during an erase operation with the drain region, the source region and the control gate connected to ground, and a relatively high potential applied to the erase gate, stored electrons are removed from the floating gate to the erase gate through the Fowler-Nordheim tunneling process (see col. 7, lines 14-17 and col. 7, lines 28-40).

Claim Rejections - 35 USC § 103

➢ The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein

were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

- Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Eitan et al. (US Patent No. 4,998,220) in view of Chang (US Patent No. 6,125,060).

Regarding claim 10, Eitan et al. fail to teach an erase gate overlapping the floating gate. However, Chang teaches that is well known in the art to extend the erase gate (122) to cover portions of the control gate (101) and the floating gate (103) (see Fig. 1F). Therefore, it would have been obvious to one having ordinary skill in the art at the same time the invention was made to modify Eitan et al. to include an erase gate that overlaps portions of the floating gate and the control gate. The ordinary artisan would have been motivated to modify Eitan et al. in the manner described above for at least the purpose of manufacturing a semiconductor device having low currents for both program and erase operations.

Allowable Subject Matter

- Claims 1-2 and 16-17 are allowed.

- The following is a statement of reasons for the indication of allowable subject matter: the prior art fails to teach, disclose, or suggest, either alone or in combination, a semiconductor device comprising: a substrate having a channel region defined thereon,

a first insulating layer disposed over said channel region and over at least a portion of said substrate, a floating gate having at least a substantial portion thereof disposed over said channel region and separated therefrom by said first insulating layer, said floating gate having at least two side walls and a top surface; a second insulating layer disposed over said side walls and over said top surface of said floating gate, a control gate having a first portion disposed over a portion of said channel region and being separated therefrom by said second insulating layer, a second portion formed over a first one of said side walls and a third portion formed over at least a first portion of said top surface of said floating gate and being separated from said floating gate by said second insulation layer, said second portion having a surface substantially parallel to and opposing said first side wall, an erase gate formed over a second one of said side walls and over at least a second portion of said top surface of said floating gate and being separated from said second one of said side walls and said portion of said top surface of said floating gate by said second insulation layer, a drain formed in a portion of said substrate proximate said control gate, and a source region formed in a portion of said substrate proximate said erase gate.

Response to Arguments

➢ Applicant's arguments about claims 8-10, filed December 28, 2002, have been fully considered but they are not persuasive. With regards to Applicant's arguments about the functional "whereby" statement, Applicant should note that it has been held that the functional "whereby" statement does not define any structure and

accordingly cannot serve to distinguish. *In re* Mason, 114 USPQ 127, 44 CCPA 937 (1957). Thus, the functional limitation of how the structure operates, as argued by Applicant, does not constitute a limitation in any patentable sense. As such, the rejection is considered to be proper.

Conclusion

➢ The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following reference is related to the present invention: Kao et al. (US Pat. No. 6,274,436 B1). The following references disclose a similar structure: Figure 2G of Lin et al. (US Pat. No. 6,355,527 B1), Figures 1-2 of Van Houdt et al. (US Pat. No. 6,246,612 B1), and Figure 10A of Kim et al. (US Pat. No. 5,821,143).

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R Díaz whose telephone number is (703) 308-6078. The examiner can normally be reached on 9:00-5:00 Monday, Tuesday, Thursday and Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (703) 308-1690. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 746-3891 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

JRD
March 7, 2003

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800